In the Claims:

1. (Currently Amended) A semiconductor ~~memory chip~~ device comprising:

a plurality of wells of a first conduction type, each well formed in a substrate and containing a first set of active components and a first set of contacts associated with the first set of active components; and

a plurality of wells of a second conduction type, each well formed in a substrate and containing a second set of active components and a second set of contacts associated with the active components,

wherein the wells of the first conduction type share a mutually adjoining boundary with the wells of the second conduction type, the mutually adjoining boundary disposed within a border region, wherein a contamination zone due to implantation scattering during well implantation lies within the border region;

wherein the first set of contacts and second set of contacts lie in the border region near the mutually adjoining boundary, and

wherein the active components lie further away from the mutually adjoining boundary than do the first and second set of contacts.

2. (Currently Amended) The ~~memory chip~~ semiconductor device of claim 13 ~~claim 1~~, wherein the memory chip comprises a DRAM chip.

3. (Currently Amended) The ~~memory chip~~ semiconductor device of claim 1, wherein the wells of the first conduction type and the wells of the second conduction type are arranged in a circuit layout structure that is ~~structures are~~ not mirror-symmetrical with respect to a center line

therein.

4. (Currently Amended) The ~~memory chip~~ semiconductor device of claim 2, wherein the wells of the first conduction type and the wells of the second conduction type are arranged in a circuit layout structure that is ~~structures are~~ not mirror-symmetrical with respect to a center line therein.

5. (Currently Amended) The ~~memory chip~~ semiconductor device of claim 3, wherein the wells of the first conduction type are p-type, and each include at least one n-channel FET ~~FETs~~ fabricated thereon, and

wherein the wells of the second conduction type are n-type, and include at least one p-channel FET ~~FETs~~ fabricated thereon.

6. (Currently Amended) The ~~memory chip~~ semiconductor device of claim 4, wherein the wells of the first conduction type are p-type, and each include at least one n-channel FET ~~FETs~~ fabricated thereon, and

wherein the wells of the second conduction type are n-type, and include at least one p-channel FET ~~FETs~~ fabricated thereon.

7-9. (Canceled)

10. (Currently Amended) A ~~DRAM memory chip architecture~~ semiconductor chip comprising:

a plurality of pairs of wells, each pair including an n-type well adjacent to a p-type well, wherein a border region is defined along an edge where each n-well and p-well are mutually adjacent;

a set of contacts within each well arranged to lie within the border region; and

a set of active components within each well arranged to lie outside the border region;

wherein the arrangement of the pairs of wells is such that there is no mirror symmetry of the well location with respect to a line through the center of the chip; and

wherein a contamination zone due to implantation scattering during well implantation lies within the border region within each pair of wells.

11-12. (Canceled)

13. (New) The semiconductor chip of claim 10, wherein the semiconductor chip comprises a memory chip.

14. (New) The semiconductor chip of claim 13, wherein the semiconductor chip comprises a DRAM chip.

15. (New) The semiconductor device of claim 1, wherein the device comprises a memory chip.

16. (New) The semiconductor device of claim 1, wherein the active components lie outside the border region.

17. (New) A semiconductor device comprising:

a plurality of pairs of wells, each pair including an n-type well adjacent to a p-type well, wherein a border region is defined along an edge where each n-well and p-well are mutually adjacent, wherein a contamination zone due to implantation scattering during well implantation lies within the border region within each pair of wells;

at least one contacts within each well arranged to lie within the border region; and

at least one active component within each well arranged to lie outside the border region.

18. (New) The device of claim 17, wherein the semiconductor device comprises a memory chip.

19. (New) The device of claim 18, wherein the semiconductor device comprises a DRAM chip.

20. (New) The device of claim 17, wherein no active components lie within the border region within each well.

21. (New) The device of claim 17, wherein the pairs of wells are arranged such that there is no mirror symmetry of the well location with respect to a line through the center of a region that includes the wells.